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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,576	11/12/2003	Tongbi Jiang	2269-4886.1US (01-0201.01)	6662
24247	7590	02/21/2006		EXAMINER
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110				DOLAN, JENNIFER M
			ART UNIT	PAPER NUMBER
				2813

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No.	Applicant(s)	
	10/706,576	JIANG ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 30 January 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

a) The period for reply expires _____ months from the mailing date of the final rejection.
 b) The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
 (a) They raise new issues that would require further consideration and/or search (see NOTE below);
 (b) They raise the issue of new matter (see NOTE below);
 (c) They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
 (d) They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: See Continuation Sheet. (See 37 CFR 1.116 and 41.33(a)).

4. The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
 5. Applicant's reply has overcome the following rejection(s): none.
 6. Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
 7. For purposes of appeal, the proposed amendment(s): a) will not be entered, or b) will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: none.

Claim(s) objected to: none.

Claim(s) rejected: 1-22.

Claim(s) withdrawn from consideration: none.

AFFIDAVIT OR OTHER EVIDENCE

8. The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
 9. The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

10. The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. The request for reconsideration has been considered but does NOT place the application in condition for allowance because:
See Continuation Sheet.

12. Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____

13. Other: _____.

- Continuation of 3. NOTE: The new limitation of a "substantially rigid" substrate in claim 18 as well as the cancellation of some claimed embodiments in claim 1 would require further search and consideration.

Continuation of 11. does NOT place the application in condition for allowance. Insofar as the Applicant's arguments can be applied to the 9/6/05 claimset and the 11/30/05 rejection (i.e., all arguments pertaining to the electrical connections as required in the 1/30/06 amendment or the rigid substrate as introduced in the 1/30/06 amendment will not be discussed in the following section), the arguments are responded to as follows:

Regarding the Shimada reference, the Applicant argues that the back side of the chip 11 is located above an upper surface of the rigid insulator board. This is not persuasive for at least the reason that figure 6, cited in the 11/30/05 Office Action, clearly shows a top side of the chip at or above the top of the rigid insulator board and the back side substantially coplanar with the substrate. Alternatively, in figure 4c, it is not apparent which side of the chip is to be considered the "back side." Hence, the bottom side of the chip substantially coplanar with the bottom of the substrate can be taken as the "back side."

Regarding the Urushima reference, the Applicant argues that one third of the thickness of the chip is located outside of the plane in which the lower surface of the interposer is located. This is not persuasive, because "substantially coplanar" is not standardly defined as being within any specific percentage or specific dimension, but rather, absent any specific definition or guidelines provided in the disclosure as to the metes and bounds of 'substantially,' it has been held to be a broad term (see *In re Nehrenberg* 280 F.2d 161, 126 USPQ 383 (CCPA 1960). Since any approximations of the difference in planarity appear to derive solely from taking measurements of figure 11A (the examiner would consider the difference about one fifth of the thickness of the chip, as opposed to one-third), and hence have no real value as differences in coplanarity, and since the bottom of the chip and the substrate appear in figure 11A to be approximately or generally coplanar, it is the Examiner's opinion that the degree of planarity in figure 11A falls under the broad umbrella of "substantially coplanar."

Regarding Washida, the Applicant argues that the bottom chip cannot be considered to be "over" the bottom surface of the interposer substrate. The Examiner generally agrees with this interpretation. Washida is applied primarily for claim 20, which requires a step of electrically connecting the bond pads of the first and second chips through the receptacle, wherein the electrically connecting step includes securing a conductive structure to at least one bond pad of the first or second device, and wherein the securing occurs before positioning the first or second devices. If the electrically connecting step "includes" the securing step, then it is reasonable to assume that the electrically connecting step is also conducted before the positioning step. Since the Examiner does not see how such a situation would be physically possible other than by connecting the chips and inserting the smaller chip into the hole (as is depicted in figures 7 and 8 of the present Application), the Examiner has interpreted claims 18-20 as being the embodiment of figures 7 and 8, which are not dissimilar to the teachings in Washida. If the Applicant intends to claim a method including a securing step, then a positioning step, and then the electrically connecting step, the Examiner recommends amending claim 19 such that the electrically connecting step is not recited as "including" a securing step.

The remaining arguments appear to be based upon the 1/30/06 amended material, and thus will not be treated.



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PRIMARY EXAMINER